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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/773,502	02/02/2001	Keiichi Kusumoto	10873.644US01	3298

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Merchant & Gould P.C.
P.O. Box 2903
Minneapolis, MN 55402-0903

EXAMINER
PATEL, PARESH H

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 08/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/773,502	Applicant(s) KUSUMOTO, KEIICHI	
	Examiner Paresh Patel	Art Unit 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) *1-19 and 25-43* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-24 and 44-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of Species 5 (Claims 20-24 and 44-48) in Paper No. 6 is acknowledged. \ fig. 11

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20-24 and 44-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (fig. 16-17) in view of Gray (US 5793126).

Regarding claims 20 and 44, Applicant's admitted prior art (hereafter APA) discloses: a semiconductor device [4' of fig. 16] having a semiconductor integrated circuit [chip of fig. 16], the semiconductor device comprising:

a first internal line [a line between PD1 and DU of fig. 16] provided within the semiconductor integrated circuit;

a first internal terminal [PD3 of fig. 16] and a second internal terminal [PD1 of fig. 16] provided within the semiconductor integrated circuit;

a first external line [a line between 1' and L3 of fig. 16] provided outside the semiconductor integrated circuit;

a second external line [a line between 1' and L1 of fig. 16] provided outside the semiconductor integrated circuit and connected to the first internal line;

a first connection [W3 of fig. 16] for connecting the first external line and the first internal terminal;

a second connection [W1 of fig. 16] for connecting the first external line and the second internal terminal.

APA discloses all the essential element of the claimed invention except for a first switch connected between the first internal terminal and the first internal line; and a second switch connected between the second internal terminal and the first internal line.

Gray discloses a first switch [Qn of fig. 2] connected between the first internal terminal [one end of 70] and the first internal line [line between 60-62]; and a second switch [Qn+1] connected between the second internal terminal [one end of 71] and the first internal line [line between 60-62]. Gray also discloses closing the first switch [via Qn] while opening the second switch [Qn+1 or Qn+2]; applying an inspection signal [from 120] from the first external line [line of 30] to the second external line [line of 32] ; and inspecting a connection state between the first external line and the first internal terminal at the first connection.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of APA with switches of Gray, in order to test continuity of bond wire [see abstract and lines 55-59 of column 2].

Regarding claims 21 and 45, Gray discloses: within the semiconductor integrated circuit [10] a switch controlling section [24] for controlling opening and closing of the first and second switches.

Regarding claims 22 and 46, Gray discloses a power source terminal [one end of 30 of 10] of the switch controlling section is connected to an internal power source line connected to a power source line [line 30 of fig. 1] provided outside the semiconductor integrated circuit; a grounding terminal [ground terminal of 10 fig. 1] of the switch controlling section is connected to an internal grounding line connected to a grounding line [line between ground and terminal of 10 of fig. 1] provided outside the semiconductor integrated circuit; and at least one of the internal power source line and the internal grounding line is separated from the first internal line [see fig. 1-2].

Regarding Claims 23 and 47, Gray discloses: a power source terminal [one end of 30 of 10] of the switch controlling section is connected to the first internal line; and a grounding terminal [ground terminal of 10 fig. 1] of the switch controlling section is connected to an internal grounding line connected to a grounding line provided outside [line between ground and terminal of 10 of fig. 1] the semiconductor integrated circuit.

Regarding Claims 24 and 48, Gray discloses: a grounding terminal [ground terminal of 10 fig. 1] of the switch controlling section is connected to the first internal line; and a power source terminal [one end of 30 of 10] of the switch controlling section is connected to an internal power source line connected to a power source line provided outside [line of 30 of fig. 1] the semiconductor integrated circuit..

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 703-306-5859. The examiner can normally be reached on M-F (8:30 to 4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 703-308-1680.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Paresh Patel
July 28, 2002

7/29/02

MICHAEL SHERRY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800